AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A current cell comprising:

a first transistor coupled to an output of the current cell and to a first input of the current cell;

a second transistor coupled in series with the first transistor and coupled to a bias input; and

a third transistor having a gate and a substrate coupled to a gate and a substrate of the second transistor, respectively, and a drain and a source coupled to a second input of the cell.

2. (Original) The current cell of claim 1, having a gate of the first transistor coupled to the first input, a drain of the first transistor coupled to the output, a source of the first transistor coupled to a drain of the second transistor, and a source of the second transistor coupled to a ground.

3. (Original) The current cell of claim 1, wherein the second input of the current cell is configured to receive a signal that is a compliment of the first signal received at the first input.

4. (Original) The current cell of claim 1, wherein the first transistor is configured as a switching transistor, and the second transistor is configured as a current source.

5. (Original) The current cell of claim 1, further comprising:

a resistor coupled between the gates of the second and third transistors and the bias input.

6. (Original) The current cell of claim 1, wherein each of the first, second, and third transistors are at least one of N-type MOSFETs and P-type MOSFETs.

7. (Original) An apparatus comprising a plurality of current cells, wherein each current cell includes:

a first transistor configured as a switching transistor, the first transistor is coupled to an output and to a first input configured to receive a first signal;

a second transistor coupled in series with the first transistor, the second transistor is configured as a current control transistor and is coupled to a bias input; and

a third transistor having a gate and a substrate coupled to a gate and a substrate of the second transistor, respectively, and a drain and a source coupled to a second input configured to receive a second signal that is a compliment of the first signal.

8. (Original) The apparatus of claim 7, wherein the plurality of current cells are coupled in parallel at respective outputs and bias inputs and the plurality of cells are coupled to a plurality of digital signals at respective first and second inputs.

9. (Original) The apparatus of claim 7, wherein each cell further includes:

a resistor coupled between a gate of the second transistor and the bias input.

10. (Currently Amended) The apparatus of claim 7, wherein the apparatus comprises at least one of a digital to analog converter, wave-shaper, controlled current source, ~~and~~ pulse generator, a microprocessor, a computer system, a network interface device, a bus interface, and a single ended digital signal driver.

11. (Currently Amended) A current cell comprising:

a first transistor of a current cell coupled to ~~an~~ a common output of a plurality of current ~~cell~~ cells and the first transistor coupled to a first input of the current cell;

a second transistor of the current cell coupled in series with the first transistor; and

a third transistor of the current cell coupled between a bias input of the current cell and a gate of the second transistor, a gate of the third transistor is coupled to a second input of the current cell.

12. (Currently Amended) The circuit of claim 11, having a gate of the first transistor coupled to the first input, a drain of the first transistor coupled to the output, a source of the first transistor coupled to a drain of the second transistor, a source of the second transistor ~~couple~~ coupled to a ground, a drain of the third transistor coupled to the bias input, and a source of the third transistor coupled to the gate of the second transistor.

13. (Currently Amended) The circuit of claim 11, further comprising:

logic configured to generate a first signal and a second signal, wherein the second signal ~~that~~ goes HIGH after the first signal goes HIGH, the second signal goes LOW before the first signal goes LOW and, the first signal is coupled to the first input and the second signal is coupled to the second input.

14. (Currently Amended) The apparatus of claim 13, wherein the logic comprises:

a first, a second, a third and a fourth inverter coupled in a series configuration; and

a NOR gate having a first gate input coupled to an output of the fourth inverter and a second gate input coupled to an input of the first inverter and to a reference signal, wherein the first signal is generated at a node coupling an output of the third inverter to an input of the fourth inverter and wherein the second signal is generated by an output of the NOR gate.

15. (Original) The circuit of claim 11, wherein the first, second, and third transistors are at least one of N-type MOSFETs and P-type MOSFETs.

16. (Currently Amended) An apparatus comprising at least one current cell, each current cell including:

a first transistor configured as a switching transistor, the first transistor coupled to ~~an~~ a common output of each of the current cells and to a first input configured to receive a first signal;

a second transistor coupled in series with the first transistor, the second transistor configured as a current control transistor; and

a third transistor configured as a switching transistor between a bias input and a gate of the second transistor, the third transistor coupled to a second input configured to receive a second signal.

17. (Currently Amended) The apparatus of claim [[17]] 16, wherein the apparatus comprises at least one of a digital to analog converter, wave-shaper, controlled current source, ~~and~~ pulse generator, a microprocessor, a computer system, a network interface device, a bus interface, and a single ended digital signal driver.

18. (Currently Amended) The apparatus of claim [[18]] 17, wherein the single ended digital signal driver comprises a B-class driver.

19. (Currently Amended) The apparatus of claim [[17]] 16, wherein each cell is coupled to logic configured to generate a first signal and a second signal, wherein the second signal goes high after the first signal goes high and wherein the second signal goes low before the first signal goes low and wherein the first signal is coupled to the first input and the second signal is coupled to the second input.

20. (Original) A method of controlling a current source comprising:

receiving a first signal that controls a first switching transistor, wherein the first switching transistor is coupled to an output;

receiving a bias signal that controls a second transistor configured as a current source, wherein the second transistor is coupled in series with the first transistor; and

receiving a second signal that is a compliment of the first signal, wherein the second signal is coupled to a drain and a source of the third transistor and wherein a gate and a substrate of the third transistor are coupled to a gate and a substrate of the second transistor, respectively.

21. (Currently Amended) The method of claim [[21]] 20, further comprising:

coupling a plurality of current cells in parallel at respective outputs and bias inputs, wherein each current cell includes first, the second and the third transistors and inputs to receive bias, first and second input signals and an output.

22. (Currently Amended) The method of claim [[22]] 21, further comprising:

receiving a plurality of digital signals at first and second inputs of the plurality of cells.

23-24. (Canceled)

25. (Original) A method of controlling a current source comprising:

receiving a first signal that controls a first transistor, the first transistor being coupled between an output and a second transistor; and

receiving a second signal that turns ON a third transistor after the first signal turns ON the first transistor and turns OFF the third transistor before the first signal turns OFF the first transistor, the third transistor being coupled between a gate of the second transistor and a bias voltage input.

26. (Currently Amended) The method of claim [[26]] 25, further comprising:

coupling a plurality of current cells in parallel at respective outputs and bias inputs, wherein each current cell includes the first, the second and the third transistors and inputs for receiving a bias, first and second input signals and an output.

27. (Currently Amended) The method of claim [[27]] 26, further comprising:

receiving a plurality of digital signals at respective first and second inputs of the plurality of cells.

28. (Currently Amended) The method of claim [[26]] 25, further comprising:

generating the first signal and the second signal from a reference signal.

29. (Currently Amended) The method of claim [[26]] 25, wherein the first, second and third transistors are at least one of N-type and P-type MOSFETs.

30. (New) An electronic system comprising:

a network interface device to communicate with network devices;

a die having a plurality of current cells, one of the current cells including:

a first transistor coupled to an output of the current cell and to a first input of the current cell;

a second transistor coupled in series with the first transistor and coupled to a bias input; and

a third transistor having a gate and a substrate coupled to a gate and a substrate of the second transistor, respectively, and a drain and a source coupled to a second input of the cell.

31. (New) The electronic system of claim 30, wherein a gate of the first transistor is coupled to the first input, a drain of the first transistor is coupled to the output, a source of the first transistor is coupled to a drain of the second transistor, and a source of the second transistor is coupled to a ground.

32. (New) The electronic system of claim 30, wherein the second input of the one current cell is configured to receive a signal that is a compliment of the first signal received at the first input.

33. (New) The electronic system of claim 30, wherein the first transistor is configured as a switching transistor, and the second transistor is configured as a current source.

34. (New) The method of claim 20, wherein the first second and third transistors are N-type MOSFETs.

35. (New) The method of claim 20, wherein the first, second and third transistors are P-type MOSFETs.

36. (New) The method of claim 22, wherein the first, second and third transistors are N-type MOSFETs.

37. (New) The method of claim 22, wherein the first, second and third transistors are P-type MOSFETs.